

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

### Listing of Claims:

1           1. (Previously Amended) A semiconductor device  
2 including an input circuit or an output circuit configured  
3 with a plurality of first MOS transistors in a first area  
4 of a principal plane on a semiconductor substrate, and an  
5 internal circuit configured with a plurality of second MOS  
6 transistors in a second area of the principal plane on the  
7 semiconductor substrate,  
8           wherein a first voltage is applied to said plurality  
9 of first MOS transistors,  
10           wherein a second voltage smaller than said first  
11 voltage is applied to said plurality of second MOS  
12 transistors,  
13           wherein a gate length of a first gate electrode of  
14 said plurality of first MOS transistors is larger than a  
15 gate length of a second gate electrode of said plurality of  
16 second MOS transistors, and

17            wherein a spacing between said first gate electrode of  
18   the first MOS transistors and a first contact hole for  
19   connecting a wiring to a source region or a drain region of  
20   the first MOS transistors is larger than a spacing between  
21   said second gate electrode and a second contact hole for  
22   connecting a wiring to a source region or a drain region of  
23   the second MOS transistors.

1            2.   (Previously Amended) A semiconductor device  
2   including an input circuit or an output circuit configured  
3   with a plurality of first MOS transistors in a first area  
4   of a principal plane on a semiconductor substrate, and an  
5   internal circuit configured with a plurality of second MOS  
6   transistors in a second area of the principal plane on the  
7   semiconductor substrate,

8            wherein a first voltage is applied to said plurality  
9   of first MOS transistors,

10           wherein a second voltage smaller than said first  
11   voltage is applied to said plurality of second MOS  
12   transistors,

13           wherein a gate length of a first gate electrode of  
14   said plurality of first MOS transistors is larger than a

15 gate length of a second gate electrode of said plurality of  
16 second MOS transistors, and

17 wherein a spacing between an edge of a first active  
18 region in which the first MOS transistors are formed and a  
19 first contact hole for connecting a wiring to a source  
20 region or a drain region of the first MOS transistors is  
21 larger than a spacing between an edge of a second active  
22 region in which the second MOS transistors are formed and a  
23 second contact hole for connecting a wiring to a source  
24 region or a drain region of the second MOS transistors.

1 3. (Previously Amended) A semiconductor device  
2 according to Claim 1,  
3 wherein said input circuit or said output circuit  
4 operates with said first voltage, and  
5 wherein said internal circuit operates with said  
6 second voltage.

1 4. (Previously Amended) A semiconductor device  
2 according to Claim 1,  
3 wherein said plurality of first MOS transistors are  
4 first voltage withstanding MOS transistors, and

5            wherein said plurality of second MOS transistors are  
6    second voltage withstanding MOS transistors.

1            5.    (Previously Amended) A semiconductor device  
2    according to Claim 1,  
3            wherein a gate insulating film thickness of the first  
4    MOS transistors is larger than a gate insulating film  
5    thickness of the second MOS transistors.

1            6.    (Previously Amended) A semiconductor device  
2    according to Claim 1,  
3            wherein an area of the active region in which the  
4    first MOS transistors are formed is larger than an area of  
5    the active region in which the second MOS transistors are  
6    formed.

1            7.    (Previously Amended) A semiconductor device  
2    according to Claim 1,  
3            wherein said plurality of first MOS transistors are p-  
4    channel type, and the source of each of said plurality of  
5    first MOS transistors is supplied with said first voltage,  
6    and

7            wherein said plurality of second MOS transistors are  
8   p-channel type, and the source of each of said plurality of  
9   second MOS transistors is supplied with said second  
10   voltage.

8-20 (Cancelled)

1            21. (Previously Amended) A semiconductor device  
2   according to Claim 2,  
3            wherein said input circuit or said output circuit  
4   operates with said first voltage, and wherein said internal  
5   circuit operates with said second voltage.

1            22. (Previously Amended) A semiconductor device  
2   according to Claim 2,  
3            wherein said plurality of first MOS transistors are  
4   first voltage withstanding MOS transistors, and  
5            wherein said plurality of second MOS transistors are  
6   second voltage withstanding MOS transistors.

1            23. (Previously Amended) A semiconductor device  
2   according to Claim 2,

3            wherein a gate insulating film thickness of the first  
4 MOS transistors is larger than a gate insulating film  
5 thickness of the second MOS transistors.

1            24. (Previously Amended) A semiconductor device  
2 according to Claim 2,

3            wherein an area of the active region in which the  
4 first MOS transistors are formed is larger than an area of  
5 the active region in which the second MOS transistors are  
6 formed.

1            25. (Previously Amended) A semiconductor device  
2 according to Claim 2,

3            wherein said plurality of first MOS transistors are p-  
4 channel type, and the source of each of said plurality of  
5 first MOS transistors is supplied with said first voltage,  
6 and

7            wherein said plurality of second MOS transistors are  
8 p-channel type, and the source of each of said plurality of  
9 second MOS transistors is supplied with said second  
10 voltage.

26. (Cancelled)